## WE CLAIM

1. Apparatus for processing data, said apparatus comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain or a non-secure domain, said plurality of modes including:

at least one secure mode being a mode in said secure domain; and

at least one non-secure mode being a mode in said non-secure domain;

wherein

when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode;

said processor includes a non-secure translation table base address register operable in said non-secure domain to indicate a region of memory storing non-secure domain memory mapping data defining how virtual addresses are translated to physical addresses within said non-secure domain; and

said processor includes a secure translation table base address register operable in said secure domain to indicate a region of memory storing secure domain memory mapping data defining how virtual addresses are translated to physical addresses within said secure domain.

2. Apparatus as claimed in claim 1, wherein non-secure domain memory mapping data is non-secure domain memory page table data and secure domain memory mapping data is secure domain memory page table data.

3. Apparatus as claimed in claim 1, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode said plurality of exception vector is performed via said monitor mode.

4. Apparatus as claimed in claim 3, wherein when in said monitor mode said processor does not use virtual memory addressing.

5. Apparatus as claimed in claim 1, wherein said non-secure translation table base address register and said secure translation table base address register are not writable when said processor is in said non-secure domain.

6. Apparatus as claimed in claim 1, wherein said non-secure translation table base address register and said secure translation table base address register exception control register are part of a configuration controlling coprocessor couple to said processor.

7. Apparatus as claimed in claim 1, wherein said processor is responsive to an exception condition to select an exception handler in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition, said active exception vector table being one of a plurality of exception vector tables and different exception vector tables being selected for use by virtue of being mapped into a predetermined region of virtual memory by a currently active one of said non-secure domain memory mapping data and said secure domain memory mapping data.

8. A method of processing data, said method comprising the steps of:

executing a program with a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain or a non-secure domain, said plurality of modes including:

at least one secure mode being a mode in said secure domain; and

at least one non-secure mode being a mode in said non-secure domain; wherein

when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode;

said processor includes a non-secure translation table base address register operable in said non-secure domain to indicate a region of memory storing non-secure

domain memory mapping data defining how virtual addresses are translated to physical addresses within said non-secure domain; and

said processor includes a secure translation table base address register operable in said secure domain to indicate a region of memory storing secure domain memory mapping data defining how virtual addresses are translated to physical addresses within said secure domain.

9. A method as claimed in claim 8, wherein non-secure domain memory mapping data is non-secure domain memory page table data and secure domain memory mapping data is secure domain memory page table data.

10. A method as claimed in claim 8, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode said plurality of exception vector is performed via said monitor mode.

11. A method as claimed in claim 10, wherein when in said monitor mode said processor does not use virtual memory addressing.

12. A method as claimed in claim 8, wherein said non-secure translation table base address register and said secure translation table base address register are not writable when said processor is in said non-secure domain.

13. A method as claimed in claim 8, wherein said non-secure translation table base address register and said secure translation table base address register exception control register are part of a configuration controlling coprocessor couple to said processor.

14. A method as claimed in claim 8, wherein said processor is responsive to an exception condition to select an exception handler in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition, said active exception vector table

being one of a plurality of exception vector tables and different exception vector tables being selected for use by virtue of being mapped into a predetermined region of virtual memory by a currently active one of said non-secure domain memory mapping data and said secure domain memory mapping data.

15. A computer program product having a computer program operable to control a data processing apparatus in accordance with a method as claimed in claim 8.